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A MICROPROCESSOR INTERFACE FOR THE OHIO UNIVERSITY PROTOTYPE OMEGA NAVIGATION RECEIVER

A hardware interface is described which allows a microcomputer to obtain data and interrupt signals from the Ohio University Omega Receiver Prototype.

by

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I. INTRODUCTION

The Ohio University Omega Prototype Receiver is currently under final design and construction for participants in the Joint University Program in Air Transportation Systems sponsored by NASA Langley Research Center. As initially designed, digital and analog hardware outputs were provided for attachment of tape recorders or chart recording equipment for capture of Omega LOP data.

The interface described in this paper was designed to demonstrate the concept of direct microprocessor attachment to the existing receiver to allow far more flexibility of output data handling than previously provided.

The interface has been brassboarded and is operational.

II. CIRCUIT DESCRIPTION

Figure 1 illustrates the hardware required for the JOLT(TM) microcomputer interface to the Ohio University Omega Receiver Prototype. This interface allows the JOLT to select either receiver status or Omega phase data for input to memory and subsequent processing.

JOLT connector J1 provides address and data bus connection and interrupt control for the interface. In operation, the interface receives an interrupt signal once per Omega time slot after the memory-aided phase locked loop (MAPLL) has produced a phase estimate for the current time slot. Simultaneously, receiver backplane wiring contains current time slot phase data from the MAPLL (6 bits), a line which goes high during the station "A" time slot, and four lines which go high when receiver station selector switches are set to the current time slot in the Omega sequence.

The interface is organized into two memory-mapped words of read-only JOLT computer memory. The CD4002 4-input NOR gates decode the high-order four address bits from the JOLT bus, enabling backplane outputs to the JOLT for status lines if JOLT address 8XXX is addressed in a "load" operation. Phase data is enabled to the data bus if JOLT address 9XXX is addressed in a "load" operation.

As brassboarded, the time slot interrupt to the JOLT is provided on the non-maskable interrupt line (NMI). This line is edge-triggered on the negative edge. The JOLT also has a maskable (IRQ) interrupt line. However, this line is level-triggered on a logic "O" level. To use this interface with the IRQ, it may well be necessary to provide differentiation of the interrupt signal to avoid multiple interrupt problems. This need depends upon the interrupt-service routine used.

Physically, the interface uses a portion of a standard Prototype Receiver board, and can be inserted directly into one of the digital output card-cage slots in the receiver. Figure 2 gives a full-size outline drawing of the interface.

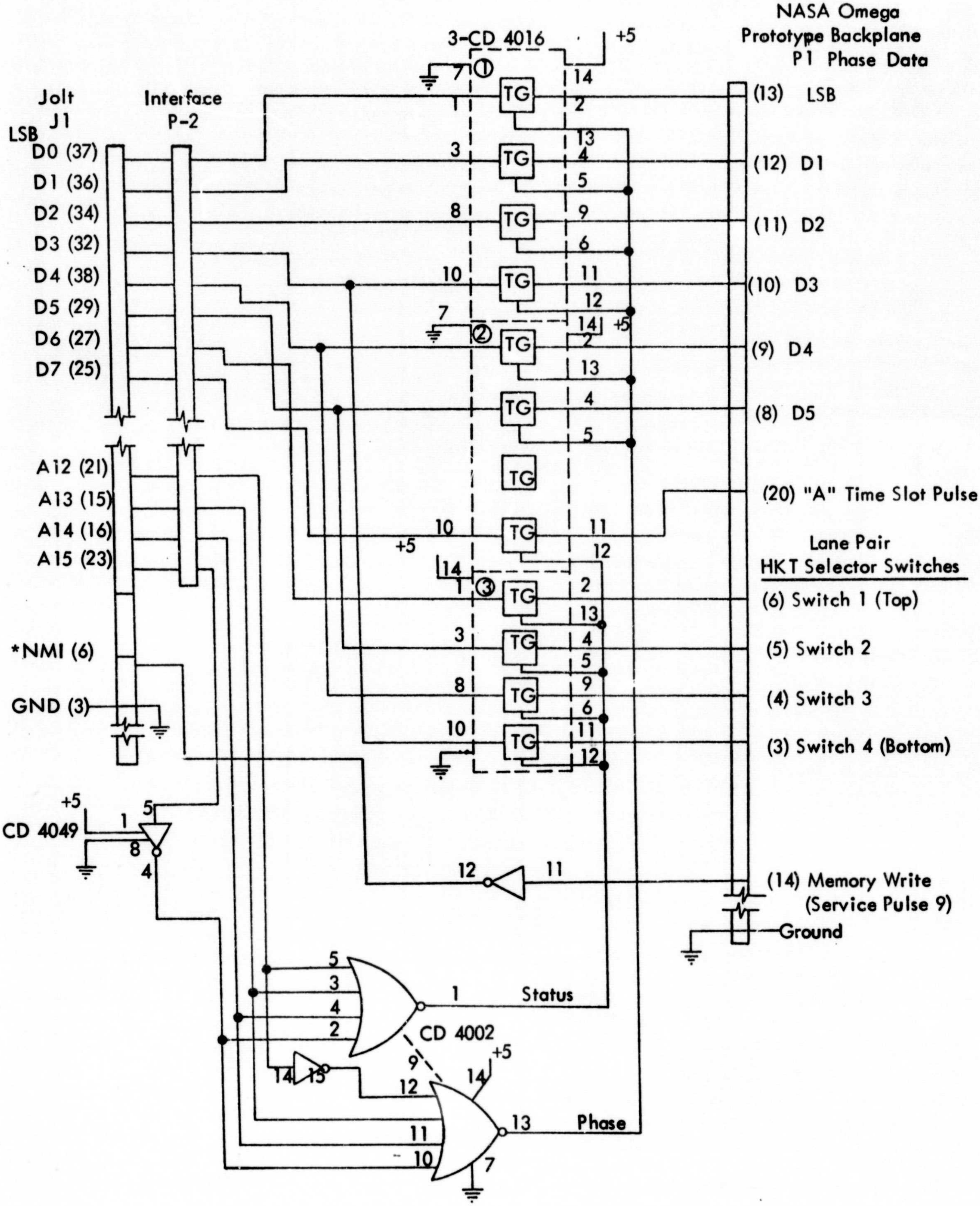


Figure 1. JOLT(TM) Interface to NASA Prototype Receivers.

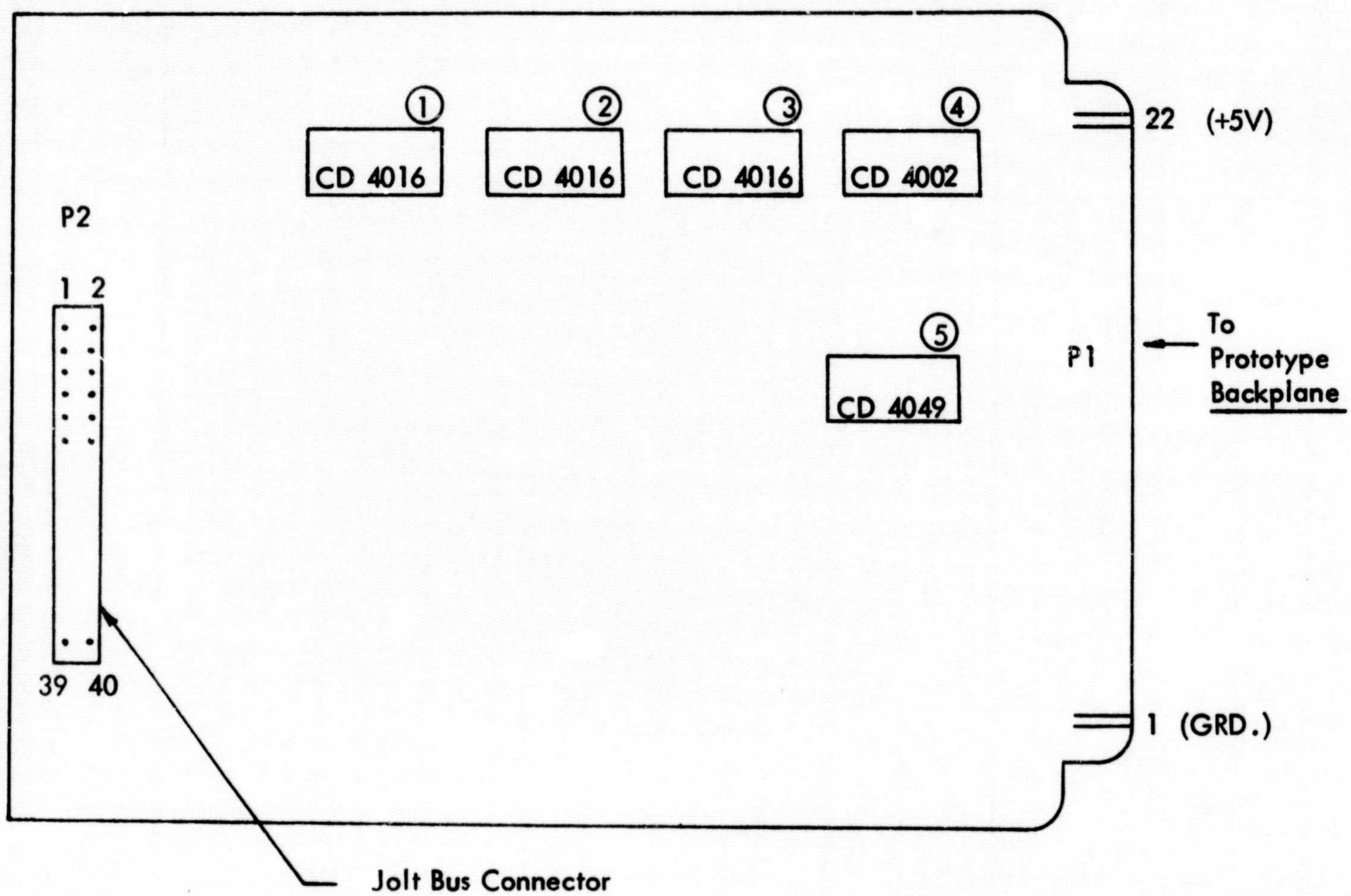


Figure 2. Jolt-to-Prototype Interface Board Component Side.

III. PROGRAMMING NOTES

The hardware interface just described provides two selectable words for input of receiver data to the JOLT microcomputer. The programmer simply codes a load operation (asking for input of data from the data bus to the accumulator or to the X or Y registers). Since the interface operates on the JOLT effective address, it will function in all appropriate addressing modes (excepting, for example, zero-page addressing since the interface is not in the zero page).

Figure 3 diagrams the functions available. If the programmer codes 8XXX as the target address of a load (for example, 8D 00 80 as a load accumulator instruction), the five high-order bits of the accumulator will be loaded (D3-D7). D7 will be a one if the current time slot which caused the interrupt was the A slot. If, for example, Switch 2 was set to station A, bit D5 would be set to one.

If the programmer desires to read Omega phase data as recorded for the current time slot by the MAPLL in the receiver, he may load accumulator from 9XXX to obtain six data bits in the low-order portion of the accumulator. He must then zero the high-order two bits, since these are not connected at all and may assume values based only on noise during the load from 9XXX.

The interface is essentially two words of read-only memory. Attempts to write on the data bus to addresses 8XXX or 9XXX will produce unpredictable results.

The interface operates in synchronization with the receiver, receiving one interrupt per receiver time slot. [1] The programmer must provide an interrupt-handling routine in order to trigger the data transfer process at such times as the receiver has valid data to be transferred. The NMI interrupt must cause the computer to read both 8XXX and 9XXX and store the results before the receiver time slot address changes. In practice, this time is long, so far as the programmer is concerned, but the data must be captured in 10 msec. or so.

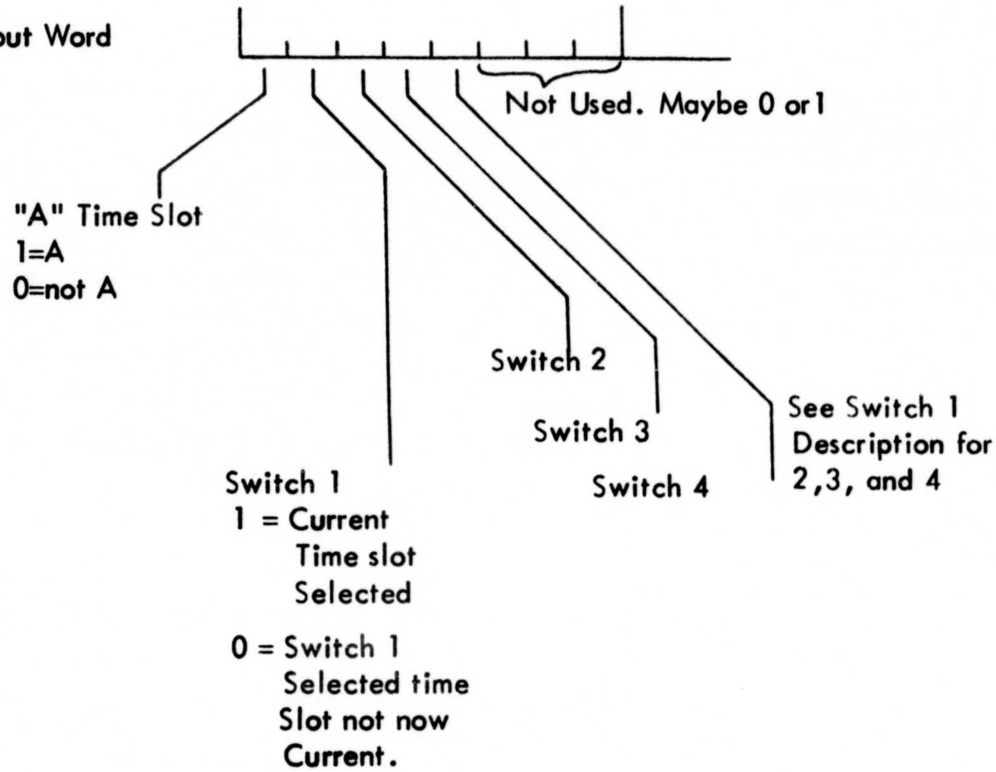
Analysis of the status byte will then allow indexed storage of the phase data in the appropriate memory location for the current Omega time slot. By determining when the A time slot occurs, the programmer can, by counting interrupts, determine when each receiver selector switch is current, thus fully determining the identification of the phase data for the two LOP's being sensed by the receiver.

IV. REFERENCES

[1] Lilley, Robert W., "Demonstration Program for Omega Receiver Prototype Microcomputer Data Processing", NASA TM No. , Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, August, 1976. (In preparation)

For Jolt Address 8XXX (Status)

Output Word



For Jolt Address 9XXX (Phase Data)

Word contains current time slot 6-bit phase from receiver.

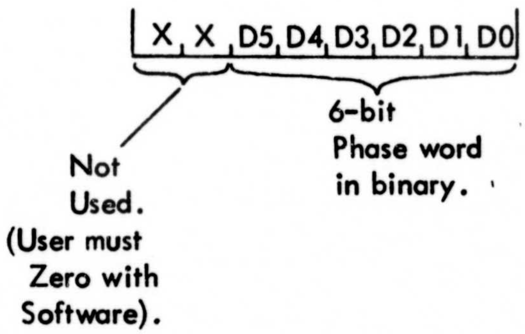


Figure 3. JOLT Interface Outputs to Software.

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